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(54) Abstract Title
Method and apparatus for process control of semiconductor fabrication

(57) A lot-base management host computer 11 performs management of wafers with a lot as a unit by managing a process condition for each lot, a correspondence between a carrier ID and a slot ID, and a correspondence between a slot ID and a wafer ID in each lot. A wafer-base management host computer 12 performs management for each wafer in a lot by managing a process condition corresponding to a wafer number in a lot. A converted-condition instructing section 13 transmits data acquired from computers 11, 12 to a semiconductor fabrication apparatus 14. The wafer-base management host computer stores a process condition for each level and a machine number of a semiconductor fabrication apparatus in the form of a matrix as an experimental level master, and issues a process condition to the semiconductor fabrication apparatus through the converted-condition instructing section according to the master for experimental levels.

FIG. 4

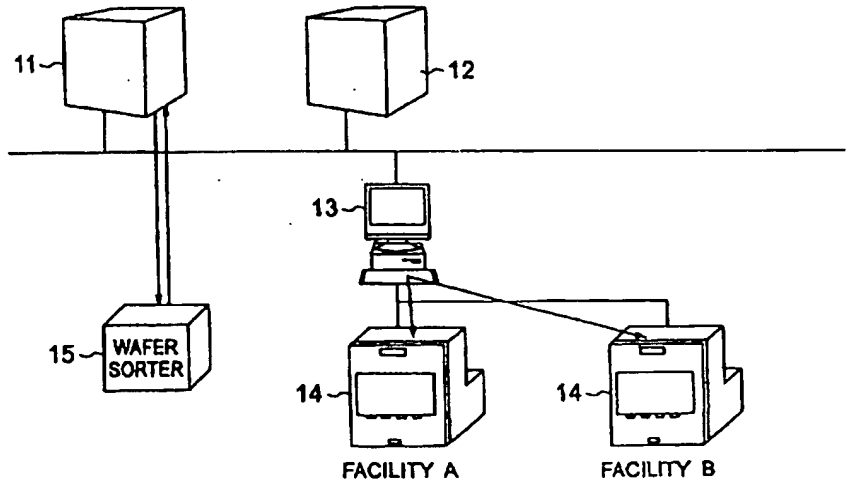

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FIG. 1
(PRIOR ART)

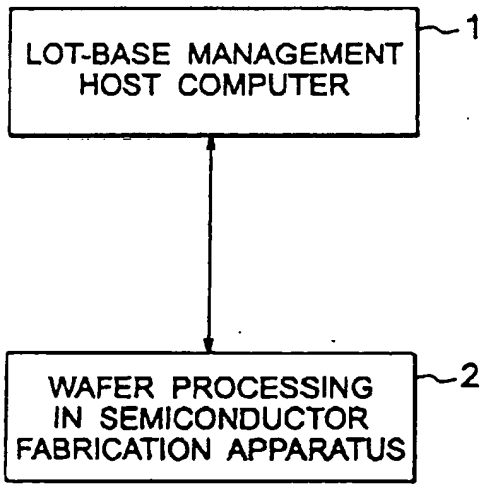


FIG. 2
(PRIOR ART)

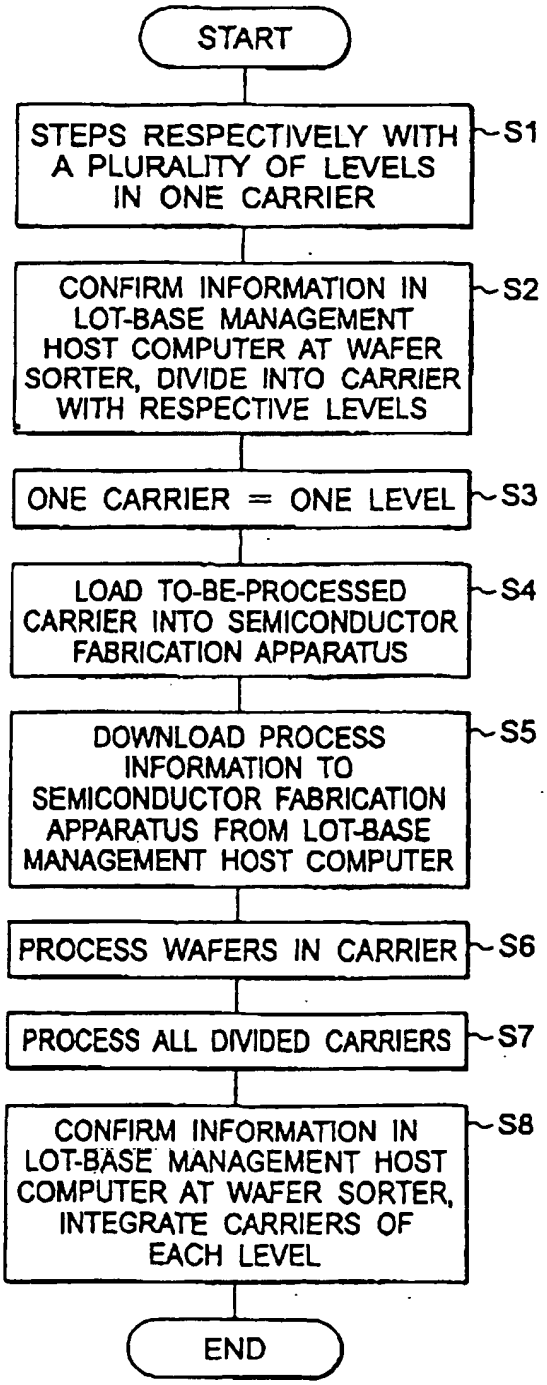


FIG. 3
(PRIOR ART)

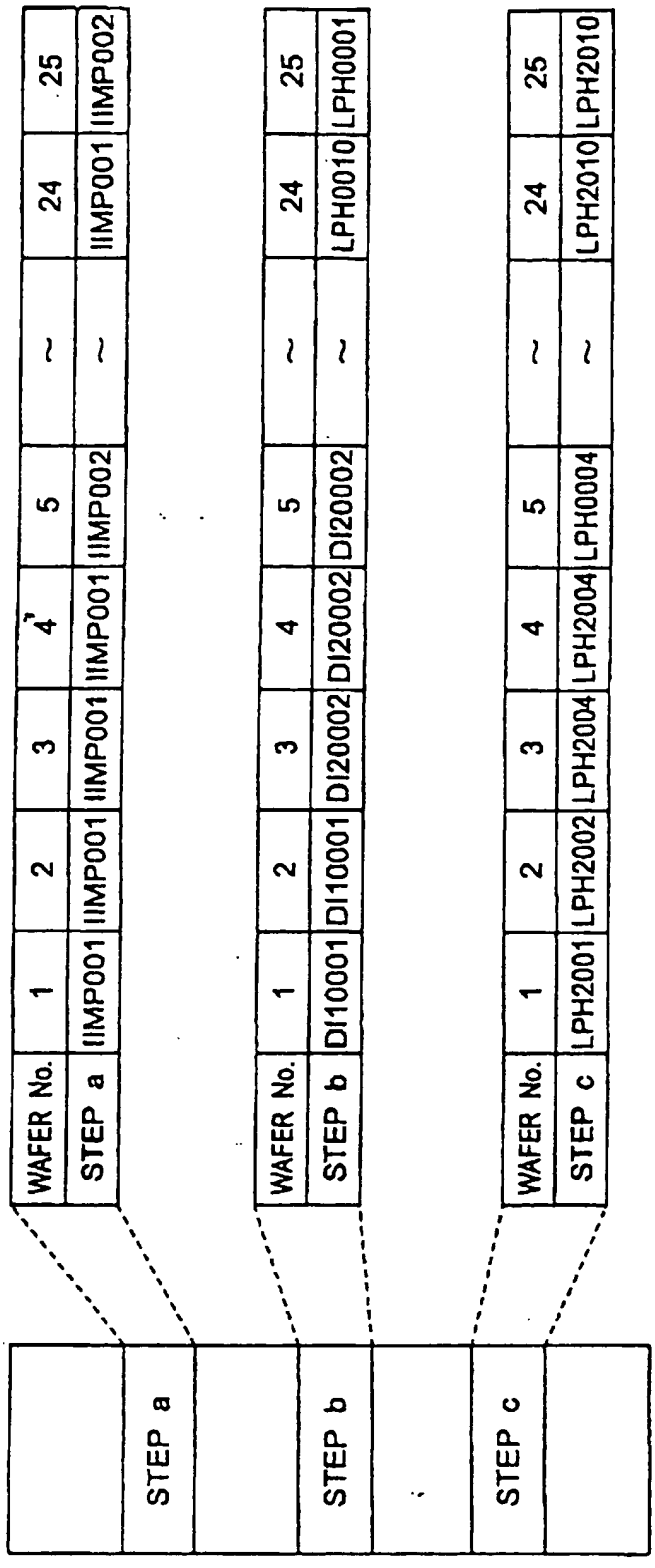


FIG. 4

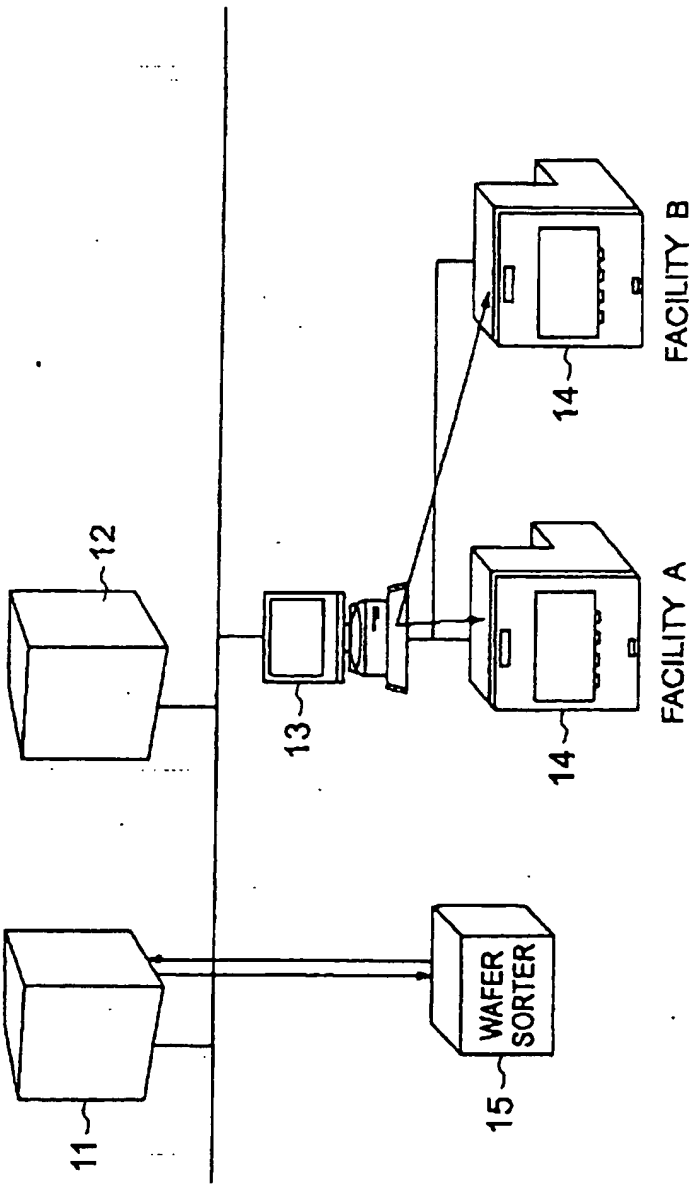


FIG. 5

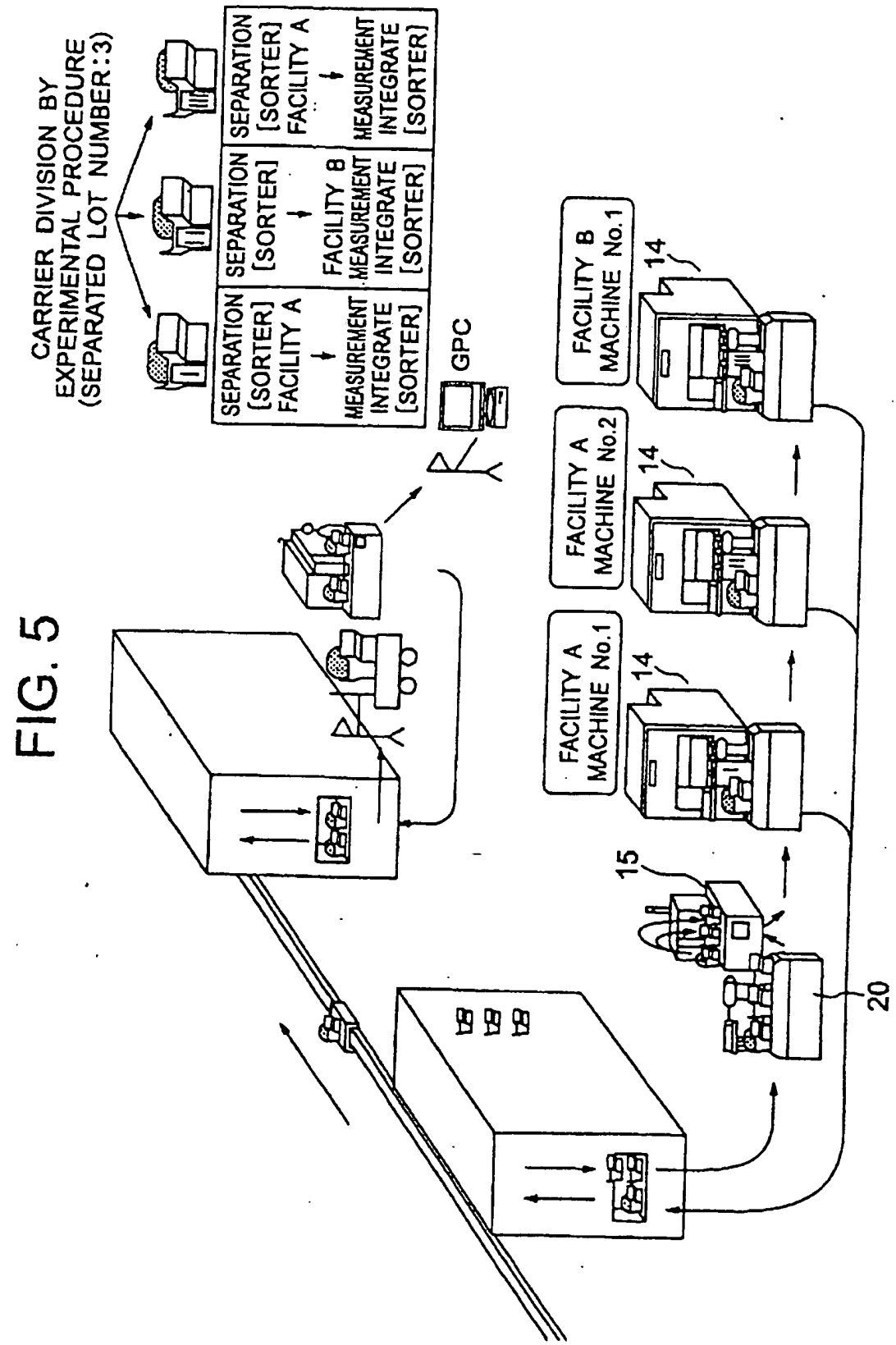

CARRIER DIVISION BY EXPERIMENTAL PROCEDURE (SEPARATED LOT NUMBER:3)
SEPARATION [SORTER] FACILITY A
MEASUREMENT INTEGRATE [SORTER]
SEPARATION [SORTER]
FACILITY B MEASUREMENT INTEGRATE [SORTER]
SEPARATION [SORTER] FACILITY A
MEASUREMENT INTEGRATE [SORTER]
GPC
FACILITY A MACHINE No.1
FACILITY A MACHINE No.2
FACILITY B MACHINE No.1
14
15
20

FIG. 6

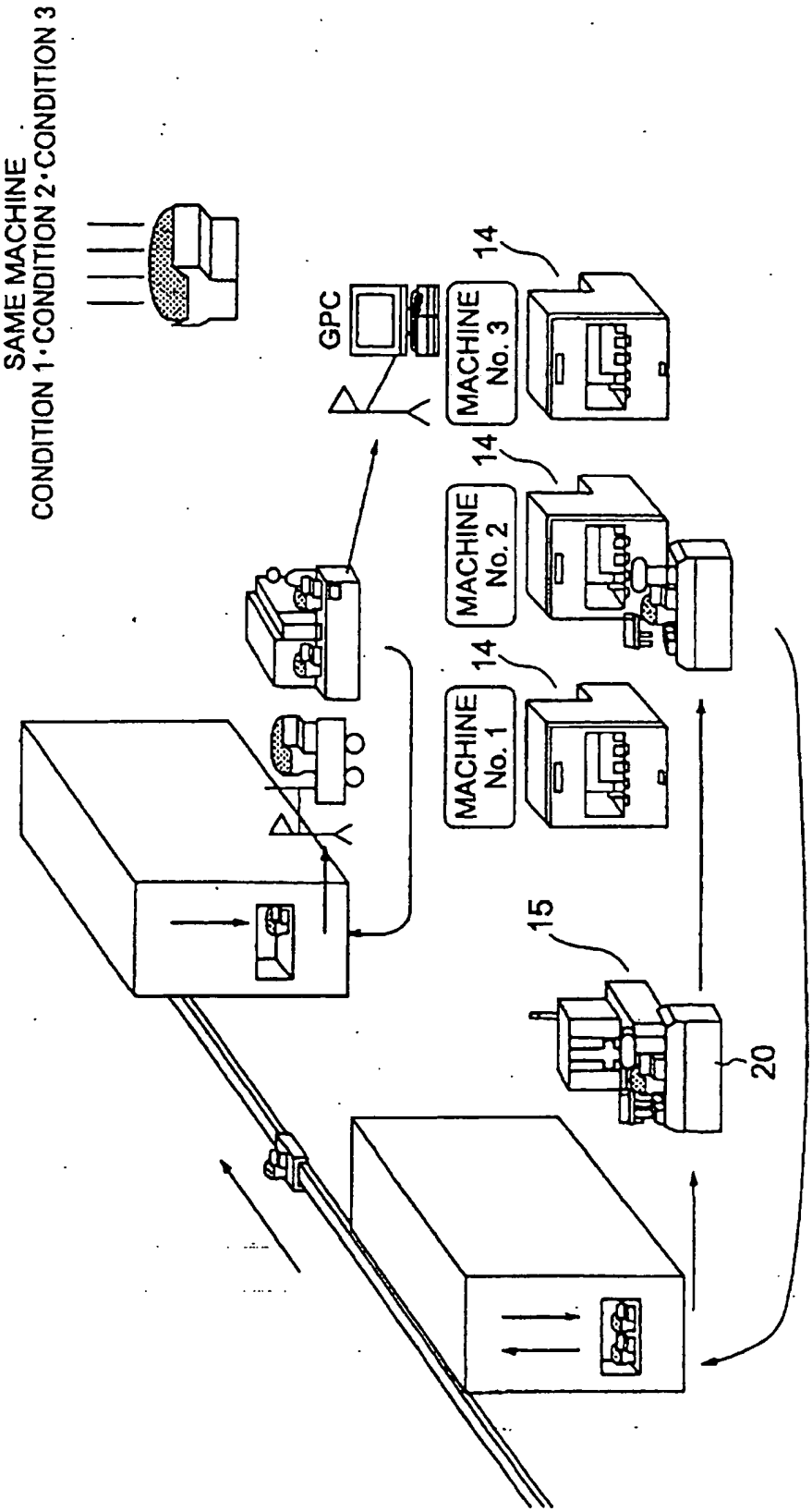
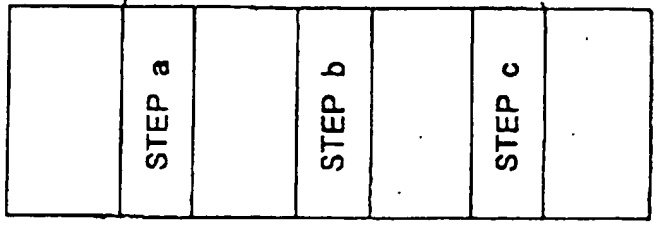
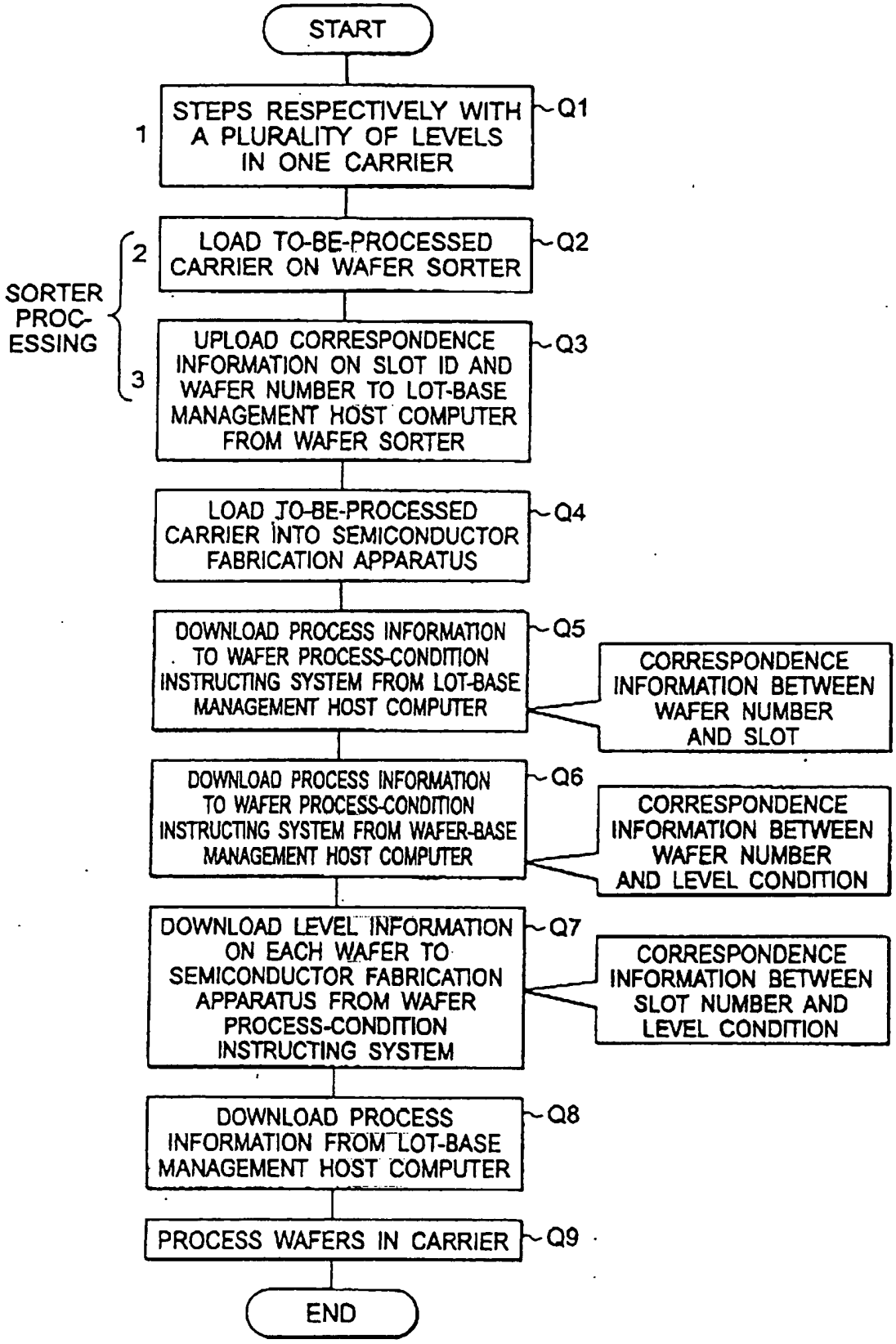

SAME MACHINE
CONDITION 1・CONDITION 2・CONDITION 3
GPC
MACHINE No. 3
MACHINE No. 2
MACHINE No. 1
14
14
14
15
20

FIG. 7



WAFER No.	1	2	3	4	5	~	24	25
STEP a	IIMP001	IIMP001	IIMP001	IIMP001	IIMP002	~	IIMP010	IIMP010
STEP b	DI10001	DI10001	DI20002	DI20002	DI20002	~	LPH0010	LPH0001
STEP c	LPH2001	LPH2002	LPH2004	LPH2004	LPH0004	~	LPH2010	LPH2010
COMPREHENSIVE LEVEL	1	2	3	3	4	~	12	13

FIG. 8


START
1
STEPS RESPECTIVELY WITH A PLURALITY OF LEVELS IN ONE CARRIER
Q1
SORTER PROCESSING
2
LOAD TO-BE-PROCESSED CARRIER ON WAFER SORTER
Q2
3
UPLOAD CORRESPONDENCE INFORMATION ON SLOT ID AND WAFER NUMBER TO LOT-BASE MANAGEMENT HOST COMPUTER FROM WAFER SORTER
Q3
LOAD TO-BE-PROCESSED CARRIER INTO SEMICONDUCTOR FABRICATION APPARATUS
Q4
DOWNLOAD PROCESS INFORMATION TO WAFER PROCESS-CONDITION INSTRUCTING SYSTEM FROM LOT-BASE MANAGEMENT HOST COMPUTER
Q5
CORRESPONDENCE INFORMATION BETWEEN WAFER NUMBER AND SLOT
DOWNLOAD PROCESS INFORMATION TO WAFER PROCESS-CONDITION INSTRUCTING SYSTEM FROM WAFER-BASE MANAGEMENT HOST COMPUTER
Q6
CORRESPONDENCE INFORMATION BETWEEN WAFER NUMBER AND LEVEL CONDITION
DOWNLOAD LEVEL INFORMATION ON EACH WAFER TO SEMICONDUCTOR FABRICATION APPARATUS FROM WAFER PROCESS-CONDITION INSTRUCTING SYSTEM
Q7
CORRESPONDENCE INFORMATION BETWEEN SLOT NUMBER AND LEVEL CONDITION
DOWNLOAD PROCESS INFORMATION FROM LOT-BASE MANAGEMENT HOST COMPUTER
Q8
PROCESS WAFERS IN CARRIER
Q9
END

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METHOD AND APPARATUS FOR PROCESS CONTROL OF SEMICONDUCTOR DEVICE FABRICATION LINE

BACKGROUND OF THE INVENTION

Technical Field

The present invention relates to a process control system that manages a plurality of semiconductor wafers as one lot, automatically issues instructions about process conditions to a fabrication facility (semiconductor fabrication apparatus), and further, collects measurement results, for example, from measuring instruments on-line. More particularly, the invention relates to a method and apparatus for process control of a semiconductor device fabrication line where input and correction of data for automatically setting levels in a plurality of experimental steps are performed with ease.

Description of the Related Art

In a semiconductor device fabrication line, there has been adopted a process control system by which fabrication facilities are not specified for respective uses in fabrication of an experimental device (a prototype product) and in fabrication of a mass fabrication device (product) in a fixed manner, but a fabrication schedule for an experimental device is incorporated in a fabrication schedule for a mass fabrication device and thus, the fabrication facilities in a single line are flexibly shared for uses in fabrication of an experimental device and in

fabrication of a mass fabrication device in a compatible manner (see, for example, JP-A 10-11108).

FIG. 1 is an illustration showing a conventional process management system of this kind in which a mass fabrication device and an experimental device are mixed. That is, a lot-base management host computer 1 is a host computer that performs management of wafers for each lot and manages process conditions for each lot, progress management for each lot, a correspondence between a carrier ID and a lot ID and a correspondence between a slot ID and a wafer ID in each lot. Further, respective semiconductor device fabrication apparatuses 2 perform various processings such as etching, ion implantation, oxide film formation and others on wafers in a lot to be processed according to conditions provided from the lot-base management host computer.

In a case of a special operational step including an experimental device, wafers in a carrier are divided such that a lot and a process condition are in a relation of one to one correspondence. In this case, a carrier in process is loaded into a semiconductor fabrication apparatus 2. The semiconductor fabrication apparatus 2 inquires of the lot-base management host computer 1 about lot information using the loaded carrier ID as a key. The lot-base management host computer 1 transmits a process condition corresponding to the lot to the semiconductor fabrication apparatus 2. The semiconductor fabrication apparatus 2 performs processing of wafers according to the instructed process

conditions, thereby completing operations over the entire lot.

On the other hand, in a case where an operation step is normal, that is only associated with a mass fabrication device, a carrier in process is at first loaded into a semiconductor fabrication apparatus 2. The semiconductor fabrication apparatus 2 inquires of the lot-base management host computer 1 about lot information using a loaded carrier ID as a key. The lot-base management host computer 1 transmits process conditions corresponding to the lot to the semiconductor fabrication apparatus 2. The semiconductor fabrication apparatus 2 performs processing of wafers according to the instructed process conditions, thereby completing operations over the entire lot.

Further, FIG. 2 is a flow chart showing a conventional process control system. At first, in a case where experimental steps with a plurality of levels are included in one carrier (step S1), carriers are divided into groups with respective levels while confirming information from the lot-base management host computer 1 at a wafer sorter (step S2). That is, the wafers are rearranged into the carriers according to levels at the sorter based on data acquired from the lot-base management host computer 1, wherein wafers are divided into the carriers with respective levels in a relation of one carrier to one level correspondence (step S3). After such a rearrangement, to-be-processed carriers are loaded into the semiconductor fabrication apparatuses (step S4). Then, processing information is downloaded on

the semiconductor fabrication apparatuses 2 from the lot-base management host computer 1 (step S5) and processing of wafers in the carriers are performed in the semiconductor fabrication apparatus (step S6). Such processings are performed on all the carriers into which wafers are rearranged according to levels (step S7). Thereafter, information of the lot-base management host computer 1 is confirmed at the wafer sorter and wafers in the carriers are integrated into the respective levels and each group of the wafers thus integrated are placed in one carrier when the wafers have been processed in the same condition (step S8).

FIG. 3 shows a conventional master for experimental levels. A case where a procedure of a lot A is such that a set of a step "a", a step b and a step c in that order is repeated a plurality of times in a serial manner is considered. In a conventional system, a master of experimental levels for a wafer number and each step is prepared and the master of experimental levels is stored in the lot-base management host computer and instructions are issued to semiconductor fabrication apparatuses based on the master for experimental levels.

However, in such a conventional technique, since a host computer has only performed management of wafers for each lot, the host computer has not been able to issue a complicated process condition as instructions. Further, when there is a plurality of process conditions within one lot, the conventional technique has problematically had poor efficiency in aspects of mandays and transportation since

one lot has to be divided into groups of wafers according to process conditions such that one condition corresponds to one lot.

The conventional technique has had further problems: As shown in FIG. 3, in a conventional system, since process condition for each wafer and specification data for measurement are dispersed over respective steps, relationship between steps cannot be integrally grasped for each wafer. In such a way, since set data for a plurality of steps constituting an experiment cannot be displayed for each wafer, there arises a necessity to enter level data into respective steps, which makes not only an overview of an experiment hard to grasp but also entering of data burdensome. Besides, since a comprehensive level that plays an auxiliary role in the grasping of the overview cannot be automatically calculated, it is a cause for generating an input error.

SUMMARY OF THE INVENTION

An object of the preferred embodiment of the invention is to provide a method and apparatus for process control of a semiconductor device fabrication line by means of which experimental levels in a plurality of steps can be grasped at a time, a process condition can be displayed for each wafer, and setting and management of experimental level data are performed with ease.

device fabrication line according to the present invention

is a method for managing fabrication in a semiconductor fabrication line, using a lot-base management host computer that performs management for each lot by managing a process condition for each lot, a correspondence between a carrier ID and a lot ID, and a correspondence between a slot ID and a wafer ID in each lot; a wafer-base management host computer that performs management for each wafer in a lot by managing a process condition corresponding to a wafer number in a lot; and a converted-condition instructing section that transmits data acquired from the lot-base management host computer and the wafer-base management host computer to a semiconductor fabrication apparatus. Said method comprises the following steps. Namely, the semiconductor fabrication apparatus inquires of the converted-condition instructing section about lot information based on a carrier ID loaded thereinto. The converted-condition instructing section acquires a process condition for the lot, slot ID information and wafer ID information from the lot-base management host computer, and in a case where wafers in process are experimental wafers, not only acquires information of each wafer in the lot from the wafer-base management host computer but also transmits a process condition corresponding to the slot ID to the semiconductor fabrication apparatus

A second process control method for a semiconductor device fabrication line according to the present invention comprises the following steps. Namely, when the semiconductor fabrication apparatus inquires of the converted-condition

instructing section about lot information based on a carrier ID loaded thereinto, then the converted-condition instructing section acquires a process condition for the lot, slot ID information and wafer ID information from the lot-base management host computer, and then, the converted condition instructing section, in a case where wafers in process are experimental wafers, not only acquires information of each wafer in the lot from the wafer-base management host computer but also transmits a process condition corresponding to the slot ID to the semiconductor fabrication apparatus.

A process control apparatus for a semiconductor device fabrication line according to the present invention comprises a lot-base management host computer that performs management for each lot by managing a process condition for each lot, a correspondence between a carrier ID and a lot ID, and a correspondence between a slot ID and a wafer ID in each lot; a wafer-base management host computer that performs management for each wafer in a lot by managing a process condition corresponding to a wafer number in a lot; and a converted-condition instructing section that transmits data acquired from the lot-base management host computer and the wafer-base host computer to a semiconductor fabrication apparatus. The wafer-base management host computer stores process conditions for respective levels and machine numbers of semiconductor fabrication apparatuses in use in the form of a matrix using experimental steps and wafer numbers as a master for experimental levels and issues a process

condition to the semiconductor fabrication apparatus through the converted-condition instructing section according to the master for experimental levels.

The process control apparatus for a semiconductor device fabrication line according to the present invention, may have a sorter that reads the ID of a wafer inserted in a slot of a carrier and transmits a slot ID and the wafer ID to the lot-base management host computer, or a sorter that reads the ID of a wafer inserted in a slot of a carrier, transmits a result of the reading to the lot-base management host computer and, when a correspondence between the slot ID and the wafer ID does not coincides with a correspondence therebetween that is stored in the lot-base management host computer, transfers the wafer to a correct lot.

Further, the master for experimental levels can include a control characteristic specification for each wafer in addition to a process condition. Still further, the present invention can comprise: display means for displaying the master for experimental levels; and correcting means for correcting a constitution of the master in display. Yet further, the present invention can comprise display means for determining and displaying the number of comprehensive levels as results of assigning levels in a plurality of experimental steps.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred features of the present invention will now be described, by way of example only, with reference to the accompanying drawings, in which:-

FIG. 1 is a block diagram showing a conventional process control system;

FIG. 2 is a flow chart showing operations of the

FIG. 2 is a flow chart showing operations of the conventional process control system;

FIG. 3 shows a illustration of a conventional master for experimental levels;

FIG. 4 is a block diagram showing a process control system for a semiconductor device fabrication line according to a first embodiment of the invention;

FIG. 5 is a pictorial illustration showing operations to assign machine numbers to respective apparatuses of a process control system for a semiconductor device fabrication line according to a second embodiment of the invention;

FIG. 6 is a pictorial illustration showing operations to assign conditions to respective apparatuses of a process control system for a semiconductor device fabrication line according to the second embodiment of the invention;

FIG. 7 is a tabular illustration showing a master for experimental levels in the second embodiment; and

FIG. 8 is a flow chart showing operations in the embodiments.

BRIEF DESCRIPTION OF THE DRAWINGS

Embodiments of the invention will be described in detail with reference to the accompanying drawings. FIG. 4 is a block diagram showing a process control system according to an embodiment of the invention. The present invention comprises, as a technical feature, a converted condition instructing section 13 that transmits a process

condition for the ID of each slot obtained by conversion of a process condition issued for the ID of each wafer in a to-be-processed lot thereto, to a semiconductor fabrication apparatus; and a wafer-base management host computer 12 that manages information on a wafer by wafer basis. That is, in FIG. 4, a lot-base management computer 11 manages a process condition for each lot, progress management for each lot, a correspondence between a carrier ID and a lot ID, a correspondence between a slot ID and a wafer ID (wafer number) in each lot and so on. The wafer-base management host computer 12 manages a process condition and so on corresponding to a wafer number in a lot. Further, a converted condition instructing section 13 performs communications between the lot-base management host computer 11, the wafer-base management host computer 12 and semiconductor fabrication apparatus 14, conversion of information and so on. Each semiconductor fabrication apparatus 14 processes a to-be-processed lot (wafers) according to instructions from the converted condition instructing section 13. A wafer sorter 15 reads the ID of a wafer inserted in a slot of a carrier and transmits the ID of the wafer together with information on correspondence with the ID of the slot to the lot-base management host computer 11. It is another possibility that the wafer sorter 15 reads the ID of a wafer and, when a correspondence of the ID of the wafer and the ID of the slot in which the wafer is inserted is different from a correspondence of the ID of the wafer and the ID of the slot provided from the

lot-base management host computer 11, takes out the wafer from the slot and reinsert the wafer into a correct slot.

Next, description will be made of operations of the system of the embodiment constructed as described above. At first, a carrier in process is loaded into the semiconductor fabrication apparatus 14. The semiconductor fabrication apparatus 14 inquires of the converted-condition instructing section 13 about lot information with the ID of a carrier that has been loaded as a key. The converted-condition instructing section 13 acquires the lot information, process condition and so on from the lot-base management host computer 11. In this stage, if a step in process is of a special operation as in a case of an experimental lot, the converted-condition instructing section 13 acquires information on each wafer in the lot from the wafer-base management host computer 12. The converted condition instructing section 13 further acquires slot ID information and wafer ID information of the lot from the lot-base management host computer 11. After completion of a series operation as described above, the converted-condition instructing section 13 transmits a process condition corresponding to the slot ID to the semiconductor fabrication apparatus 14. The semiconductor fabrication apparatus 14 progresses wafer processing according to an instructed process condition, thus completing operations of all the lot.

On the other hand, in a case where to-be-processed wafers are to be used for mass fabrication devices and

therefore, operational steps are of a normal type, when a carrier in process is loaded into the semiconductor fabrication apparatus 14, the semiconductor fabrication apparatus 14 inquires of the converted-condition instructing section 13 about lot information with the carrier ID as a key. The converted-condition instructing section 13 acquires the information on and process condition for the lot and so on from the lot-base management host computer 11. The converted-condition instructing section 13 transmits a processing condition corresponding to the lot to the semiconductor fabrication apparatus 14. The semiconductor fabrication apparatus 14 progresses wafer processing according to an instructed process condition, thus completing operations of all the lot.

In the embodiment that is constituted as described above, a correspondence data between a slot ID and a wafer ID in a to-be-processed lot is stored in the lot-base management host computer 11 in advance, an instruction of a process condition corresponding to a wafer ID is converted to a condition instruction for a slot ID at the converted-condition instructing section 13 based on the correspondence data and the converted-condition instructing section 13 issues condition instructions to the semiconductor fabrication apparatus 14.

Most semiconductor fabrication apparatuses 14 have no function of wafer recognition and when information on a wafer ID and information on a slot ID are different from each other, a wafer that has been processed is useless, even

when a condition is instructed according to a wafer ID, since the semiconductor fabrication apparatus 14 can perform processing only in response to instructions for a slot ID. Therefore, conversion is effected from a process condition for a wafer ID to a process condition for a slot ID, a converted process condition is transmitted to the semiconductor fabrication apparatus 14 and thereby, a wafer is processed according to the same process condition as a process condition for the wafer ID. In such a manner, in the embodiment, instructions of a process condition for each wafer can be issued. Further, even when a semiconductor fabrication apparatus 14 does not recognize a wafer, a process condition corresponding to a wafer ID can be issued to the semiconductor fabrication apparatus 14.

In addition, the lot-base management host computer 11 can control a process condition for a to-be-processed lot on a one-to-one correspondence basis only. Therefore, it would be necessary to divide the lot into groups of wafers such that wafers in each group have the same process condition, but in the embodiment, since a plurality of process conditions can be instructed at a time, a division of the lot into groups is not necessary. That is, additional new lots are not necessary, leading to higher transportation efficiency.

Next, a second embodiment of the invention will be described. FIGs. 5 to 7 are representations showing an automatic experimental system of the embodiment, FIG. 5 shows a way to assign machine numbers to carriers, FIG. 6 is

a schematic pictorial illustration of operations to assign process conditions to respective carriers and FIG. 7 is a schematic illustration showing a master for assigning levels in the embodiment.

The process control system of the embodiment shown in FIGs. 5 and 6 controls a plurality of semiconductor wafers in lots, automatically issues process conditions to fabrication facilities and collects measurement results from measuring instruments on-line. In the embodiment, data for automatically assigning process conditions in a plurality of experimental steps is entered with ease.

The lot-base management host computer (not shown in FIGs. 5 and 6) comprises: a progress management section in which a progress status of each lot is memorized; a step procedure master showing the order of steps of each lot and whether or not a step is experimental; an experimental level master showing process conditions for respective levels in the form of a matrix using steps (experimental steps) with respective levels and wafer numbers; and an input terminal (not shown) for entering, displaying and updating data of the experimental level master.

In FIGs. 5 and 6, the wafer sorter 15 takes out from a slot wafer 1 that is inserted in slots of a carrier 20, which has been transported, to read a bar code on the wafer with a camera in order to recognize which slot which wafer is inserted in; after the reading, the wafer 1 is reinserted to the original slot. The wafer sorter 15 transmits a corrspondence between the wafer ID and the slot

ID, both recognized, to the lot-base management host computer, or alternatively when the wafer sorter 15 recognizes that a taken-out wafer is inserted in an incorrect slot based on a correspondence between a wafer ID and a slot ID acquired from the lot-base management host computer, the wafer sorter 15 raises an alarm and the wafer 1 that has been inserted in a wrong slot is manually transferred to a correct slot.

An experimental level master shown in FIG. 7 is stored in the lot-base management host computer. An experimental level master on which the combination of steps "a", b, c and in correspondence to a wafer number; on the level master a wafer number and a process condition in each step are held in the form of a matrix is stored in the lot-base management host computer. In

the experimental level master, the same level is displayed in a case of combination of the same step and the same process condition. Therefore, in an example shown in FIG. 7, 25 wafers are processed, in which for example, a wafer number 3 and a wafer number 4 receive the same processing in the same step and, to be detailed, a process of a level 3 is applied to both wafer numbers 3 and 4. In such a manner, since there are plurality of wafers with the same levels, the number of patterns amounts to 13 kinds.

In the experimental level master, contents of processing displayed in a step "a" is of a step of ion implantation indicated by IIMP, and DI and LPH indicate a diffusion step and a low pressure CVD (LPCVD) steps in

processing of steps b and c. A sequence of figures following an alphabetical symbol indicate a detailed process condition.

A display that displays the experimental level master and an input device though which data is entered or corrected are connected to the wafer-base management host computer. Further, wafers whose process conditions in steps "a", b and c are the same are selected as at the same level on the lot-base management host computer and in turn, the same level is displayed on the display as a comprehensive level.

In the process control system of the embodiment thus constituted, a current step of a lot is grasped by a progress control section of the lot-base management host computer and judgment on whether or not the current step is an experimental step, or whether or not the current step is a normal step in which processing of a mass fabrication device is effected is based on a step-procedure master and information on the current step of a lot. Furthermore, in a case of a normal step, a process condition is instructed to the semiconductor fabrication apparatus 14 such that the lot is processed according to a process condition indicated by the step procedure.

On the other hand, in a case of an experimental step, the experimental level master (shown in FIG. 7) is retrieved using an ID of a level table described in the step of the step procedure and a step name in the label table as keys and process conditions for respective wafers are issued as

instructions to the semiconductor fabrication apparatus 14 according to the contents of the results of retrieval. Alternatively, the wafer sorter and a carrier transportation system for a carrier are instructed such that a lot is separated prior to the experimental step at the wafer sorter and after separation of the lot, instructions are issued to the semiconductor fabrication apparatuses 14 such that separate processings are performed in a plurality of apparatuses that have different machine numbers. In this case, the transportation system and the wafer sorter are again instructed such that the wafer sorter 15 is automatically synthesized back to the original lot after completion of the experiment at the wafer sorter 15.

As described above, in the embodiment, the experimental level master is displayed in the form of a table on the input terminal. In the display, level numbers of respective wafers are automatically calculated and presented after judging on which levels are assigned on which respective wafers all in one lot as a result of level assignment in a plurality of steps. With this display, an operator in an input operation can grasp a relationship between experimental steps, and input of the experimental level master and a correcting (updating) operation can be effected with great ease. Especially, when not only a process condition but a control characteristic specification are entered in an experimental level master, a control characteristic specification corresponding to a level can be set. In this case, input of a process condition in a step

of a fabrication facility and input of management characteristic in a step for a measuring instrument in a correspondence manner to each wafer can be effected with ease. When an operator in an input operation corrects the experimental level master on the input terminal, the result of correction is reflected on a table presented on the display connected to the lot-base management host computer. Further, when the operator pushes a confirmation button after confirmation of the contents of the table, the data of the table are informed to the lot-base management host computer to update the experimental level master.

In the embodiment, since the experimental level master in which process conditions for respective levels are described in the form of a matrix using an experimental step and a wafer number are provided and the experimental level master is displayed in the form of a table on the input device, therefore, experimental levels in a plurality of steps can be grasped at a single glance, thereby enabling setting and control of experimental data to be simplified.

Operations as described above will be explained with reference to a flow charge shown in FIG.8. A first state of this case is that wafers in a carrier have respective steps with a plurality of levels, and the steps are experimental (step Q1), a to-be-processed carrier is loaded on a wafer sorter 15 (step Q2) and the wafer sorter 15 reads slot IDs and wafer numbers in a corresponding manner. After the reading, the wafer sorter 15 uploads information on

correspondence between the slot IDs and the wafer numbers to the lot-base management host computer 11 (step Q3).

Following the upload, the to-be-processed carrier is loaded into the semiconductor fabrication apparatus 14 (step Q4). After the loading, processing information (correspondence information between a wafer number and a slot ID) is downloaded from the lot-base management host computer 11 on the converted-condition instructing section 13 (step Q5). Further, processing information (correspondence information between a wafer number and a level condition) is downloaded from the wafer-base management host computer 12 on the converted condition instructing section 13 (step Q6). Subsequent to the downloading, level information on each wafer as a wafer process condition (correspondence information between a slot ID and a level condition) is downloading from the converted condition instructing section 13 on the semiconductor fabrication apparatus 14 (step Q7), and process information is downloaded from the lot-base management host computer (step Q8). Thereafter, wafers in carriers receive predetermined processings in the respective semiconductor fabrication apparatuses (step Q9).

As described above, display of process conditions for respective wafers can be effected and a process condition corresponding to the ID of a wafer can further be instructed without confirmation of the process condition in a semiconductor fabrication apparatus. Furthermore, according to the invention, since a plurality of instructions can be effected, division of a lot is not necessary, thereby

increasing transportation efficiency. In addition, since, when an experimental level master is provided in the invention, experimental levels in a plurality of steps can be viewed on one screen, it is very easy to set and manage experimental level data.

While the present invention has been described in its preferred embodiments, it is to be understood that the words which have been used are words of description rather than limitation, and that changes may be made to the invention without departing from its scope as defined by the appended claims.

Each feature disclosed in this specification (which term includes the claims) and/or shown in the drawings may be incorporated in the invention independently of other disclosed and/or illustrated features.

The text of the abstract filed herewith is repeated here as part of the specification.

A lot-base management host computer performs management of wafers with a lot as a unit by managing a process condition for each lot, a correspondence between a carrier ID and a lot ID, and a correspondence between a slot ID and a wafer ID in each lot. A wafer-base management host computer performs management for each wafer in a lot by managing a process condition corresponding to a wafer number in a lot. Further, a converted-condition instructing section transmits data acquired from the lot-base management host computer and the wafer-base management host computer to a semiconductor fabrication apparatus. The

wafer-base management host computer stores a process condition for each level and a machine number of a semiconductor fabrication apparatus in use in the form of a matrix as an experimental level master, and issues a process condition as instructions to the semiconductor fabrication apparatus through the converted-condition instructing section according to the experimental level master.

CLAIMS:

1. A process control method for a semiconductor device fabrication line using: a lot-base management host computer that performs management for each lot by managing a process condition for each lot, a correspondence between a carrier ID and a lot ID, and a correspondence between a slot ID and a wafer ID in each lot; a wafer-base management host computer that performs management for each wafer in a lot by managing a process condition corresponding to a wafer number in a lot; and, a converted-condition instructing section that transmits to a semiconductor fabrication apparatus data acquired from the lot-base management host computer and the wafer-base management host computer;
said method comprising the steps of:

inquiring, by the semiconductor fabrication apparatus to the converted-condition instructing section, about lot information based on a carrier ID loaded into the semiconductor fabrication apparatus; and,

acquiring, by the converted-condition instructing section from the lot-base management host computer, a process condition for the lot, slot ID information and wafer ID information, and in a case where wafers in process are experimental wafers, not only acquiring information of each wafer in the lot from the wafer-base management host computer but also transmitting a process condition corresponding to the slot ID to the semiconductor fabrication apparatus.

2. A process control method for a semiconductor device fabrication line using: a lot-base management host computer that performs management for each lot by managing a process condition for each lot, a correspondence between a carrier ID and a lot ID, and a correspondence between a slot ID and a wafer ID in each lot; a wafer-base management host computer that performs management for each wafer in a lot by managing a process condition corresponding to a wafer number in a lot; and, a converted-condition instructing section that transmits to a semiconductor fabrication apparatus data acquired from the lot-base management host computer and the wafer-base management host computer;

said method comprising the steps of:

acquiring, by the converted-condition instructing section from the lot-base management host computer, a process condition for the lot, slot ID information and wafer ID information, when the semiconductor fabrication apparatus inquires of the converted-condition instructing section about lot information based on a carrier ID loaded into the semiconductor fabrication apparatus; and,

acquiring, by the converted-condition instructing section from the wafer-base management host computer, in a case where wafers in process are experimental wafers, information of each wafer in the lot, and transmitting a process condition corresponding to the slot ID to the semiconductor fabrication apparatus.

3. A process control apparatus for a semiconductor

device fabrication line, comprising:

a lot-base management host computer that performs management for each lot by managing a process condition for each lot, a correspondence between a carrier ID and a lot ID, and a correspondence between a slot ID and a wafer ID in each lot; and,

a wafer-base management host computer that performs management for each wafer in a lot by managing a process condition corresponding to a wafer number in a lot; and,

a converted-condition instructing section that transmits to a semiconductor fabrication apparatus data acquired from the lot-base management host computer and the wafer-base management host computer;

wherein the wafer-base management host computer stores process conditions for respective levels and machine numbers of semiconductor fabrication apparatuses in use in the form of a matrix, using experimental steps and wafer numbers as a master for experimental levels, and issues a process condition to the semiconductor fabrication apparatus through the converted-condition instructing section according to the master for experimental levels.

4. A process control apparatus for a semiconductor device fabrication line according to claim 3, further comprising:

a sorter that reads the ID of a wafer inserted in a slot of a carrier and transmits a slot ID and the wafer ID to the lot-base management host computer.

5. A process control apparatus for a semiconductor device fabrication line according to claim 3, further comprising:

a sorter that reads the ID of a wafer inserted in a slot of a carrier, transmits a result of the reading to the lot-base management host computer and, when a correspondence between the slot ID and the wafer ID does not coincide with a correspondence therebetween that is stored in the lot-base management host computer, transfers the wafer to a correct lot.

6. A process control apparatus for a semiconductor device fabrication line according to any one of claims 3 to 5, wherein the master for experimental levels can include a control characteristic specification for each wafer in addition to a process condition.

7. A process control apparatus for a semiconductor device fabrication line according to any one of claims 3 to 6, further comprising:

display means for displaying the master for experimental levels; and,

correcting means for correcting a constitution of the master in display.

8. A process control apparatus for a semiconductor device fabrication line according to any one of claims 3 to 7, further comprising:

display means for determining and displaying the number of comprehensive levels as results of assigning levels in a plurality of experimental steps.

9. A process control method for a semiconductor device fabrication line, the method being substantially as herein described with reference to and as shown in Figures 4 to 8 of the accompanying drawings.

10. A process control apparatus substantially as herein described with reference to and as shown in Figures 4 to 8 of the accompanying drawings.

Application No: GB 0005110.2
Claims searched: 1-10

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Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.R): G3N NGA9, NGL.

Int Cl (Ed.7): G05B 19/418; H01L 21/00, 21/02.

Other: ONLINE: EPODOC, JAPIO, WPI.

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
A	US 5,375,062	(MITSUBISHI DENKI KABUSHIKI KAISHA)	
A	JP05109596 A	(NEC YAMAGATA LTD) - cited from the abstract.	

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
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